PHASE SELECTION MECHANISM FOR OPTIMAL SAMPLING OF SOURCE SYNCHRONOUS CLOCKING INTERFACE DATA

Claim for Priority

This application claims priority from United States Patent Application Serial No. 60/260,593, filed on January 9, 2001, and which is hereby incorporated by reference as if fully set forth herein.

Field of the Invention

The present invention relates generally to Source Synchronous Clocking and related applications.

Background of the Invention

"Source Synchronous Clocking" (SSC) refers to a data interface between a transmitter and a receiver, where the transmitter launches data accompanied by clock, and the clock has a well defined phase with respect to the data. This type of interface is commonly found in communications equipment, such as the interface between a serializer/deserializer (SerDes) and a Framer.

In some cases, the receiver can use the transmitter clock to sample the data, provided that the phase between clock and data is property controlled. However in some cases, the receiver has its own local clock domain, at a commensurate frequency but at an unknown phase with respect to the transmitter clock. (Two clocks are deemed commensurate when the ratio of their frequencies is a rational number). In these cases the receiver must synchronize the transmitter data to the receiver clock domain. Therefore, some way of evaluating the relationship between the phase of the transmitter clock and the receiver clock is required. If multiple phases of the receiver clock are available, then the optimal phase can be chosen to accomplish the handoff of data between transmit and receive clock domains.

The transmitter clock frequency may be at the full symbol rate, where a single (e.g. falling) edge of the dock is used to sample the data, or it may be at half of this frequency, in a so-called Dual Data Rate (DDR) interface.

A need has been recognized in connection with effecting tangible improvements in the types of devices described above.

Summary of the Invention

At least one presently preferred embodiment of the present invention relates to a phase selection mechanism for the optimal sampling of data at the receiving end of a SSC interface. The receiver is allowed to choose between several phases of its local clock, to best synchronize the transmitter data to the receiver clock domain. It results in a minimum depth first in first out (FIFO) register to accomplish the handoff of transmit data from the transmit clock to the receive clock. It avoids the requirement of a delay locked loop (DLL) to bring the transmitter clock into a desired phase relationship with respect to the receiver clock. At least one embodiment of the present invention provides a solution specific to the DDR and full rate clocking mode types of SSC interface.

The present invention provides, in one aspect, a phase selection mechanism for facilitating the sampling of data, the phase selection mechanism comprising: an arrangement for interfacing with a transmitter clock; an arrangement for interfacing with at least one receiver clock; a phase sampler which ascertains the position of the transmitter clock with respect to the at least one receiver clock, whereby a suitable receiver clock for sampling data is ascertainable.

Furthermore, the present invention provides, in an additional aspect, a method of facilitating the sampling of data, said method comprising the steps of: providing an

arrangement for interfacing with a transmitter clock; providing an arrangement for inerfacing with at least one receiver clock; and ascertaining the position of the transmitter clock with respect to the at least one receiver clock, whereby a suitable receiver clock for sampling data is ascertained.

For a better understanding of the present invention, together with other and further features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, and the scope of the invention will be pointed out in the appended claims.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating a phase selection mechanism.

Figs. 2, 3 and 4 depict various timing diagrams, relating to the phase selection mechanism of Fig. 1, for a DDR mode.

Figs. 5, 6 and 7 depict various timing diagrams, relating to the phase selection mechanism of Fig. 1, for a full rate clocking mode.

Description of the Preferred Embodiments

Fig. 1 is a block diagram of one embodiment of a phase selection mechanism in accordance with the present invention.

Assume that there are four quadrature phases of receiver clock available, operating at frequency f. One may label the phases of these quadrature clocks as 0, 90, 180, and 270 degrees. Three four-way Muxes (102, 104, 106), whose select ports (SEL) are controlled by a signal named Phase_Select, and whose data ports (D0-D3 in each case) are attached to the quadrature clocks in a rotationally symmetric way, are preferably used to create signals CO, C180 and C270. The first Mux 102 creates signal CO, which will be at phase 0, 90, 180 or 270 when Phase_Select is 0, 1, 2 or 3 respectively. The second Mux 104 creates signal C180, which will be at Phase 180, 270, 0 or 90 when Phase_Select is 0, 1, 2 or 3 respectively. The third Mux 106 creates signal C270, which will be at phase 270, 0, 90 or 180 when Phase_Select is 0, 1, 2 or 3 respectively. Thus the three signals CO, C 180, and C270 have a constant phase relationship regardless of the value of Phase_Select. As Phase_Select is incremented, the absolute phases of CO, C 180 and C270 move together in 90 degree increments.

The transmitter (not shown), operating in SSC mode, may generate a clock of frequency f/2, (in DDR mode, where rising and falling clock edges allign with data edges) or frequncy f, (in full rate clocking mode, where falling edge clock edges allign

with data edges). The phase of the transmitter data and transmitter clock are unknown with respect to the receiver clocks. The transmitter data (Tx_Data) is captured by falling-edge-sensitive latches 108 (with ports D and C) clocked at C270. The transmitter clock (Tx_Clock) is fed into the data port of each of two latches 110, 112, to create two phase samples. The first phase sample, named P0, is the output of a level-sensitive latch 110 clocked by signal C0. The second phase sample, named P180, is the output of a falling-edge-sensitive latch (or flip-flop) 112 clocked by signal C180. Signals P0 and P180 are then combined at a two way XOR gate 114. In DDR mode, (Tx_mode pin asserted at '0') the output of gate 114 is re-sampled by a falling-edge-sensitive latch 120 clocked by C180, to create the signal Phase_Sample. In full rate clocking mode, (Tx_mode pin asserted at '1') signal P180 fed to latch 120 to create the Phase_Sample.

In DDR mode, the Phase_Sample signal may have three possible states depending on where the transmitter clock transitions lie with respect to C0 and C180. If Tx_Clock transitions occur while C0 is at '0' (low), then Phase-Sample will have a static value of '0'. Figures 2 and 3 (DDR mode) and Figures 5 and 6 (full rate clocking mode) show timing diagrams with this scenario. If Tx_Clock transitions occur while C0 is at '1' (high), then Phase_Sample will have a static value of '1'. This scenario is shown in Figure 4 (DDR mode) and Figure 7 (full rate clocking mode). If Tx_Clock transitions occur too near the falling edge of C0 or C180, such that the setup-hold time of one of the latches is violated,

then Phase_Sample will have a poorly defined value, perhaps fluctuating between '0' and 'l' over time. In full rate clocking mode, the same three scenarios exist, depending on the position of the falling edge transitions of Tx_Clock with respect to C0 and C180.

A state machine (not shown) preferably reads the value of Phase_Sample and slowly (i.e. over many clock cycles) responds by controlling signals Phase_Select and DC_Select. If Phase_Sample is 'l' then Phase_Select is incremented so that the clocks C0, Cl80 and C270 move forward 90 degrees in absolute phase. If Phase_Sample is '0' then Phase_Select is not changed. One can easily see that if Phase_Sample is '0' the Tx_Data transitions are kept well clear of the failing edge of C270, (always separated by more than 90 degrees in phase) thus ensuring that the data is captured cleanly. If Phase_Sample is unstable, (fluctuating between '0' and 'l') the state machine will move forward by 90 degree increments until a stable '0' is found.

One additional level-sensitive latch 118 is preferably utilized to completely synchronize the data for use with a receiver clock at (absolutely) phase 270. This latch (118) is clocked by a signal generated by a two way MUX 122 controlled by signal DC_Select. If DC_Select is 'l' then the clock is held high, and if DC_Select is '0' then the clock is operated at phase 90. DC_Select is directly coupled to Phase_Select in the state machine. When Phase_Select has the value of 0, 1, 2 or 3, DC_Select has the value of '1',

'1', '0' or '0' respectively. In this way the signal labeled "Rx_Data" is stable at the rising edge of receiver clock phase 270, regardless of the value of Phase_Select.

The Mux with input Tx_Mode, indicated at 116, is used to change the mode of operation from DDR mode, (Tx_Mode is set to '0') to full rate clocking mode, (Tx_Mode is set to '1').

It should be appreciated that, whereas Figures 2, 3 and 4 show timing diagrams for a DDR mode, Figures 5, 6, and 7 (corresponding to the scenarios contemplated in Figures 2, 3 and 4, respectively) show timing diagrams for a full rate clocking mode.

Though the present invention may find a wide variety of applications, a detailed discussion of a chip and transceiver which may employ the type of phase selection mechanisms described above, in accordance with at least one embodiment of the present invention, may be found in the article, "A Single-Chip 12.5Gbaud Transceiver for Serial Data Communication," Daniel Friedman et al., 2001 Symposium on VLSI Circuits, Kyoto, Japan, June 2001.

If not otherwise stated herein, it is to be assumed that all patents, patent applications, patent publications and other publications (including web-based

publications) mentioned and cited herein are hereby fully incorporated by reference herein as if set forth in their entirety herein.

Although illustrative embodiments of the present invention have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be affected therein by one skilled in the art without departing from the scope or spirit of the invention.